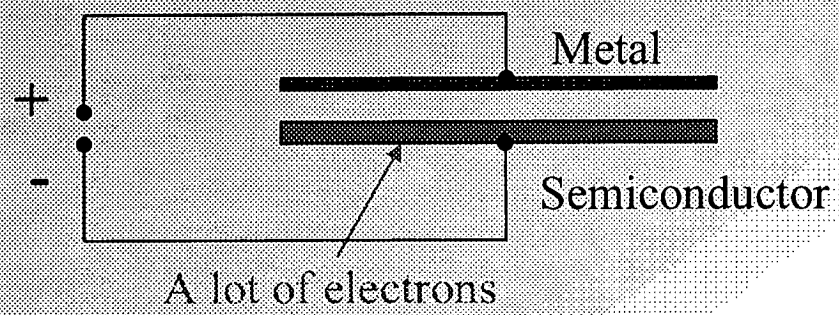
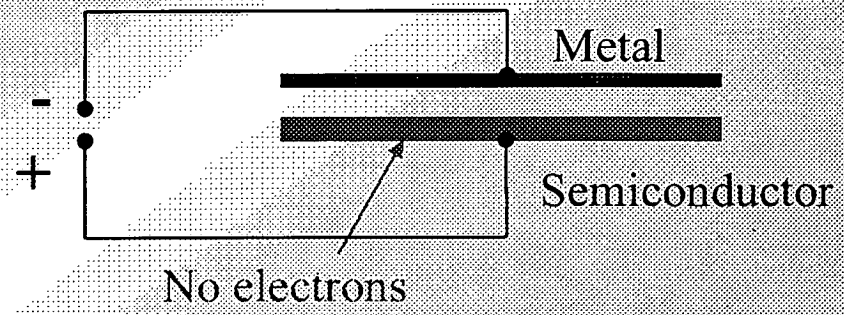
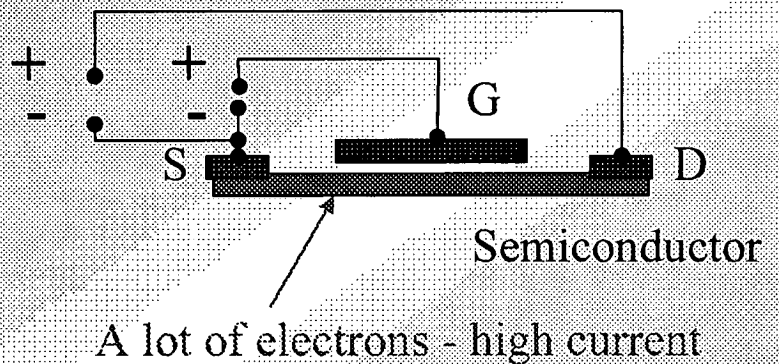
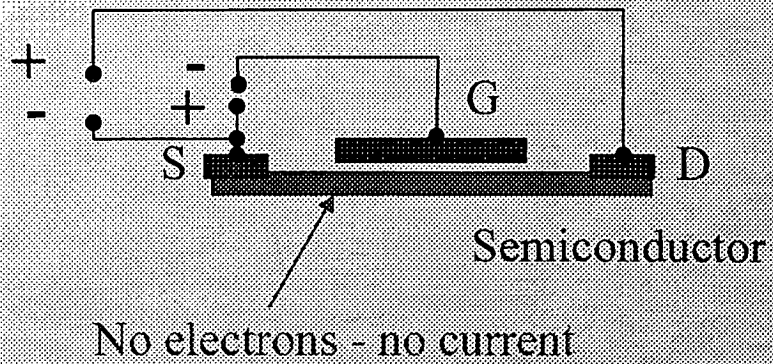
02 Field-Effect Transistor (FET) principles and types



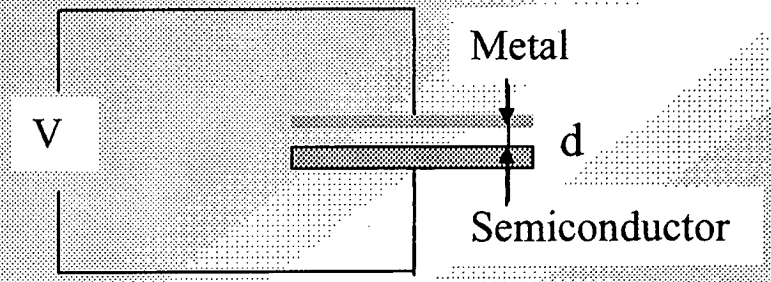






Charge control in FETs

Any FET is essentially a capacitor



Let the area of the capacitor plates be A.

The induced charge Q can be expressed as

$Q = q \times A \times \Delta n_S$,

where $q = 1.6 \times 10^{-19}$ C is the electron charge,

Δn_S is the *SURFACE CONCENTRATION* of ***induced*** electrons, $\Delta n_S = Q / (q \times A)$;

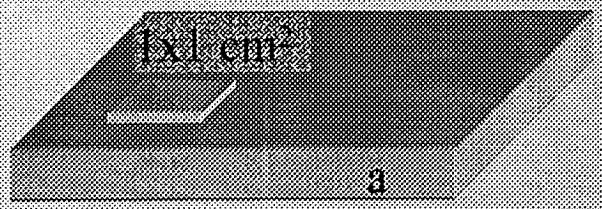
What is the surface concentration?

The bulk charge density, n

the layer thickness, a;

then the surface concentration,

$n_S = n \times a$



Estimation of induced charge

For the PLAIN CAPACITOR, $C = \varepsilon\,\varepsilon_0 \times A/d$ (ε is the dielectric permittivity of the media in the gap between the plates), d is the distance between the plates,

$$Q = C \times V = \varepsilon\,\varepsilon_0 \times A \times V/d,$$

The sign of the charges induced in the top and bottom plates are opposite. If the bottom plate is grounded, then, the induced concentration of *electrons (*which are *negatively charged)* for the *top (metal) plate:*

$$\Delta n_{SM} = -\,\varepsilon\,\varepsilon_0 \times V/(q \times d) < 0;$$

for the *bottom (semiconductor) plate*:

$$\Delta n_S = \varepsilon\,\varepsilon_0 \times V/(q \times d) > 0;$$

For a given voltage, V, the induced charge increases as we decrease d

Estimation of induced charge

Let's estimate the induced charge density

$\varepsilon = \varepsilon_r \times \varepsilon_0$; For the air gap, $\varepsilon_r = 1$; $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m;

Let d = 1 μm; V = 10 V;

Then $|\Delta n_s| = 5.53 \times 10^{14}$ m^{-2} = 5.5310^{10} cm^{-2};

If the gap between the plates is made out of dielectric, ε_r = 2 – 10 (typically), the induced concentration increases correspondingly.

In any FET type the n_S is well below ~10^{14} cm^{-2};

In metals, electron concentration $n_0 \approx 10^{23}$ cm^{-3} ;

For the metal plate only 1 μm thick, the equilibrium surface concentration:

$n_{SM} = 10^{23}$ cm^{-3} × 10^{-4} cm = 10^{19} cm^{-2} >>$|\Delta n_S|$

The threshold voltage of FETs

Suppose the semiconductor plate is doped with donors, the concentration being N_D;
The equilibrium electron concentration in the semiconductor, $n_0 = N_D$;

For the layer thickness, *a*, the surface concentration $n_{S0} = N_D \times a$;

The voltage needed to deplete the entire active layer (the semiconductor plate) is referred to as the THRESHOLD VOLTAGE of the FET

For the n-doped layer the threshold voltage is negative in order to repulse the electrons.

The induced concentration at the threshold has to compensate the equilibrium one:

$$\Delta n_{ST} = \varepsilon \varepsilon_0 \times V_T/(q \times d) = - n_{S0}$$

Therefore, $V_T = - q \times d \times n_{S0}/ (\varepsilon \varepsilon_0)$

"d" has to be LOW to obtain low threshold voltages

The threshold voltage of FETs

At the threshold the net concentration in the channel is zero:

$$\Delta n_{ST} - n_{S0} = 0;$$

If the applied voltage is above the threshold, $V > V_T$,

the net concentration can be found as:

$$n_S = \Delta n_S - \Delta n_{ST} = \varepsilon\, \varepsilon_0 /(q \times d) \times (V - V_T)$$

Note, $\varepsilon\, \varepsilon_0 /d = C_1$ the gap capacitance per unit area

Therefore,

$$\mathbf{n_S = (C_1/q) \times (V - V_T)}$$

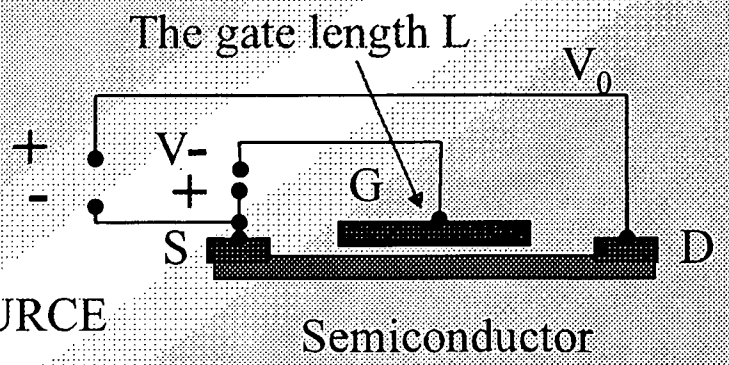
The above model is referred to as "charge control model" of FETs

FETs: general design considerations

The current through the channel is

$$I = \frac{V_0}{R}$$

where V_0 is the voltage applied between the DRAIN and the SOURCE



We are assuming that $V_0 << V_T$ (we will see why, later on)

The channel resistance, R (Z is the device width):

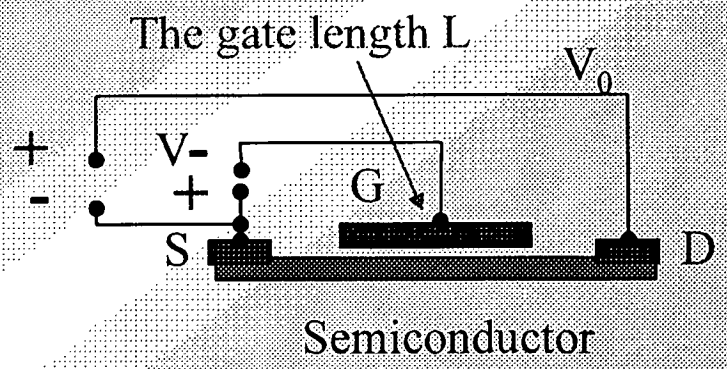
$$R = \frac{L}{q\, n\, \mu\, a Z} = \frac{L}{q\, n_s\, \mu\, Z}$$

The channel current is then: $I = V_0\, (q\, n_S\, \mu\, Z)\, /L = V_0\, q\, \mu\, Z\, (C_I/q) \times (V - V_T)\, /L$

$$\boxed{\mathbf{I = V_0\, \mu\, Z\, C_I \times (V - V_T)\, /L}}$$

FETs: general design considerations

$$I = V_0 \, \mu \, Z \, C_1 \times (V - V_T) / L$$



The transconductance, $g_m = dI/dV$;
The g_m is the "responsivity" of FET.
In the linear mode under consideration ($V_0 << V$),

$$g_m = V_0 \, \mu \, Z \, C_1 / L$$

The main factors affecting FET performance (for any FET type):

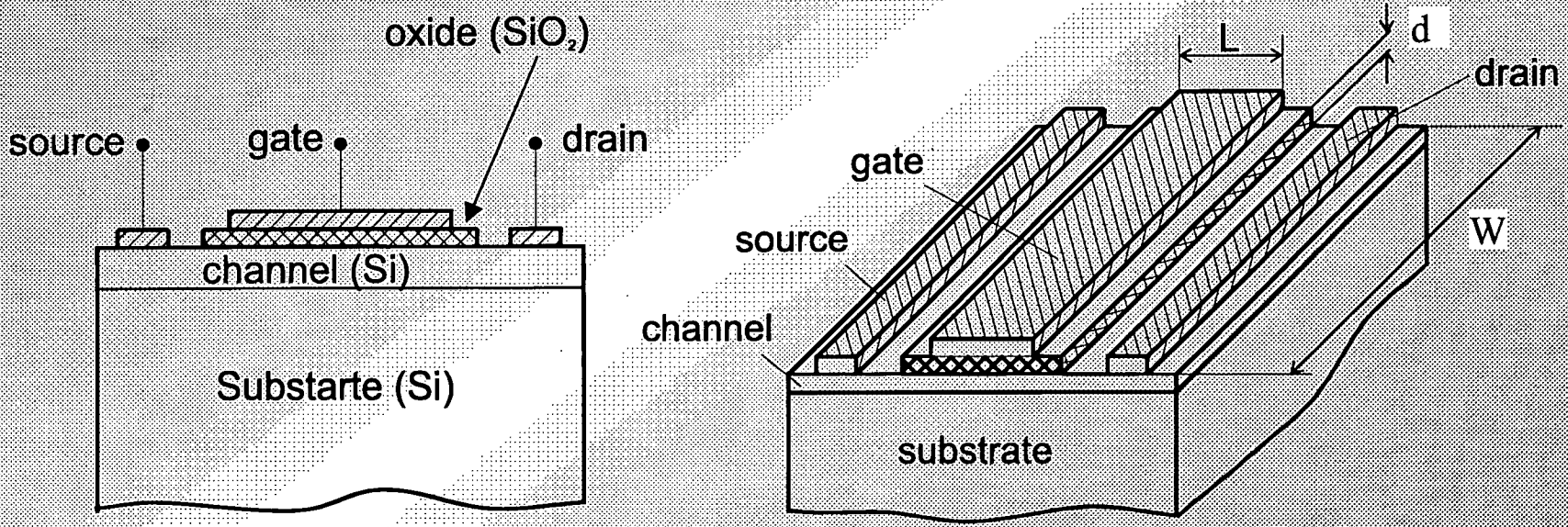
μ ↑ I and g_m ↑

L ↓ I and g_m ↑

Carrier mobility in the channel and the gate length are crucial parameters of any FET

Different FET types

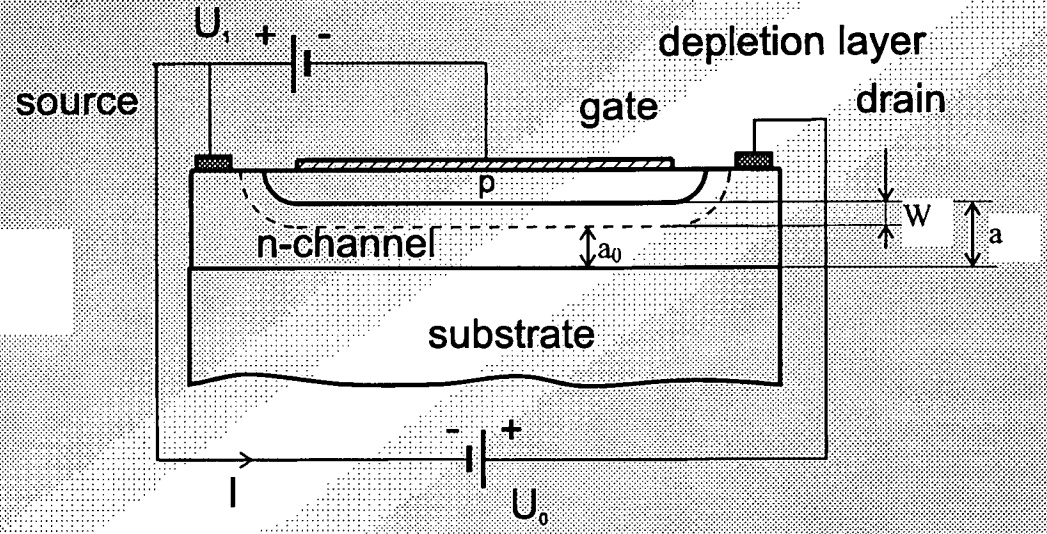
Metal - Oxide - Semiconductor FET (MOSFET)



The gate-channel insulator is made out of dielectric (SiO_2), $\varepsilon = 3.9$

Different FET types

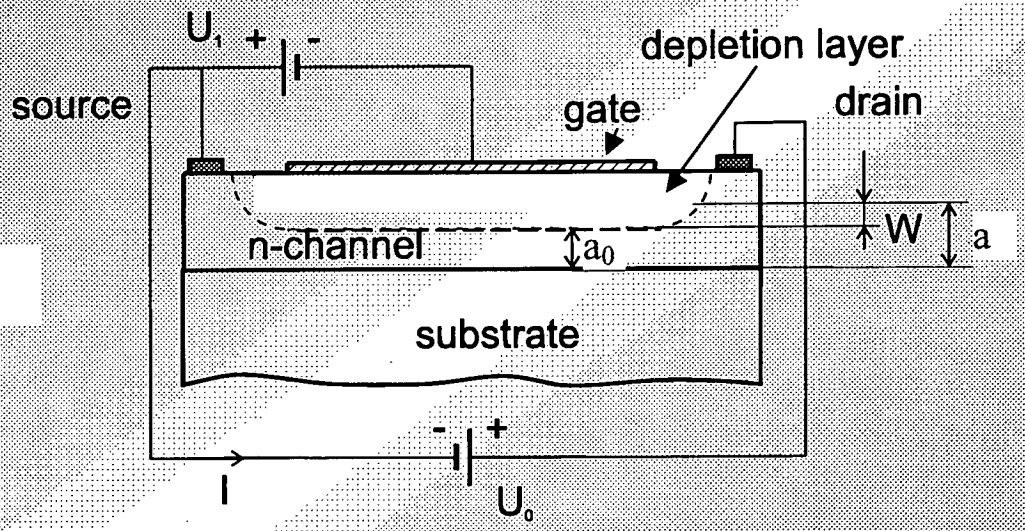
Junction FET (JFET)



The gate-channel insulator consists of the DEPLETION REGION, i.e. the same material as the channel.
For GaAs, $\varepsilon \sim 12$; for GaN $\varepsilon \sim 9$.

Different FET types

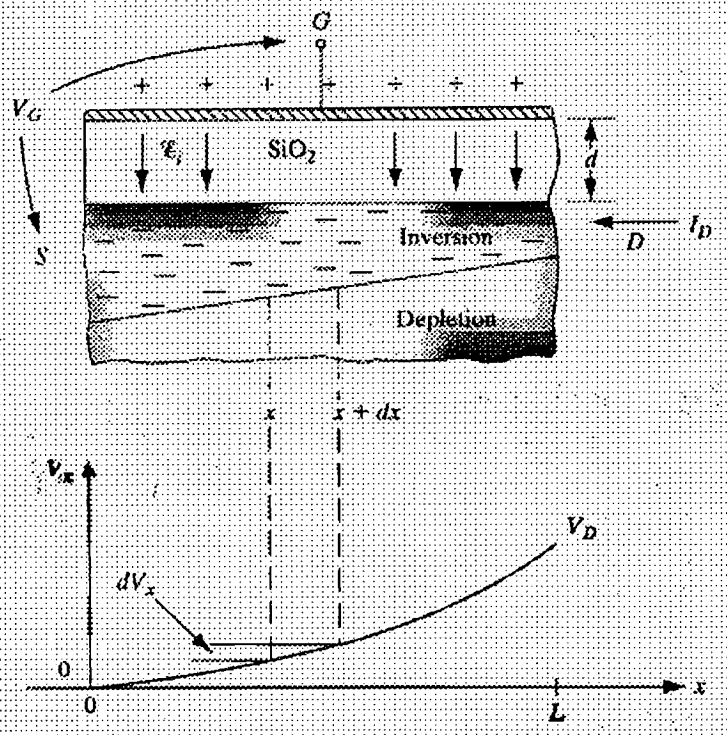
Metal-Semiconductor FET (MESFET)



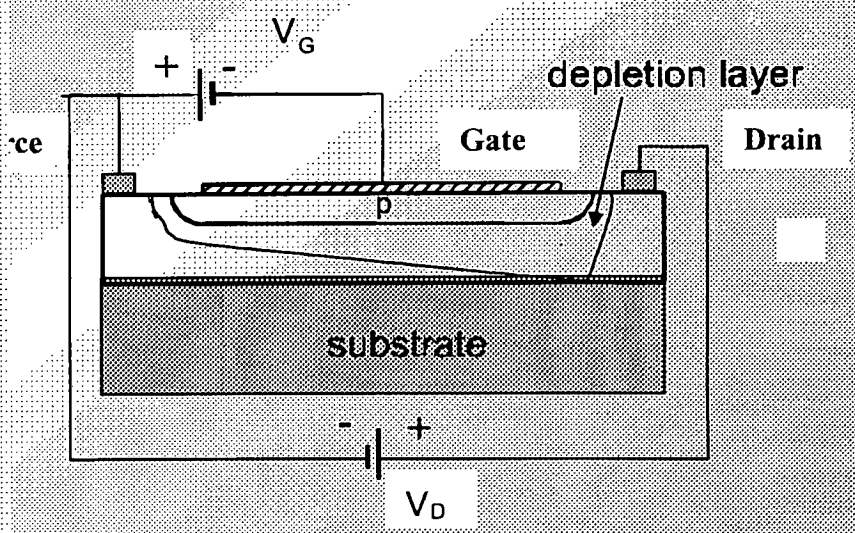
The gate is formed by Schottky barrier to the semiconductor layer. The gate-channel insulator consists of the DEPLETION REGION, i.e. the same material as the channel. Very similar to the JFET

Effects of high drain bias on FET characteristics

MOSFET

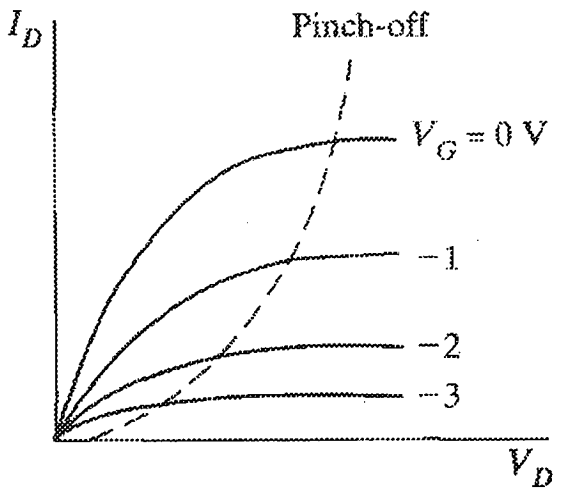


JFET



The gate- to drain voltage difference depends on the position along the gate
So does the induced charge

Effects of high drain bias on FET characteristics

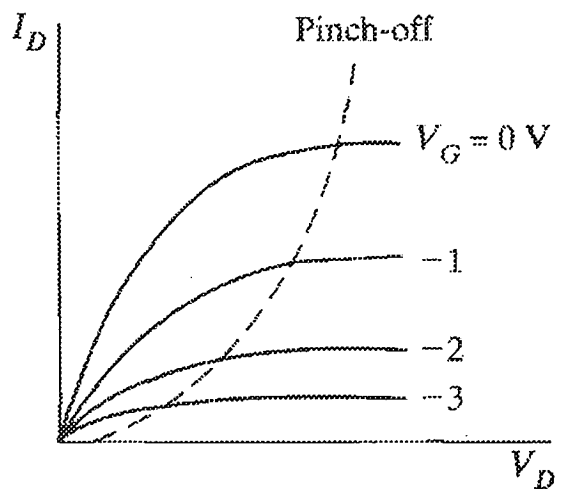


The particular range of the gate voltage depends on the device type

The channel narrowing at the drain edge of the gate causes current saturation in the FETs

Effects of high drain bias on FET characteristics

Electron velocity saturation due to high electric field in the channel



Velocity saturation due to high electric field in the channel also results in the I-V saturation

The average electric field in the channel, $E_{av} \sim V_0 / L$

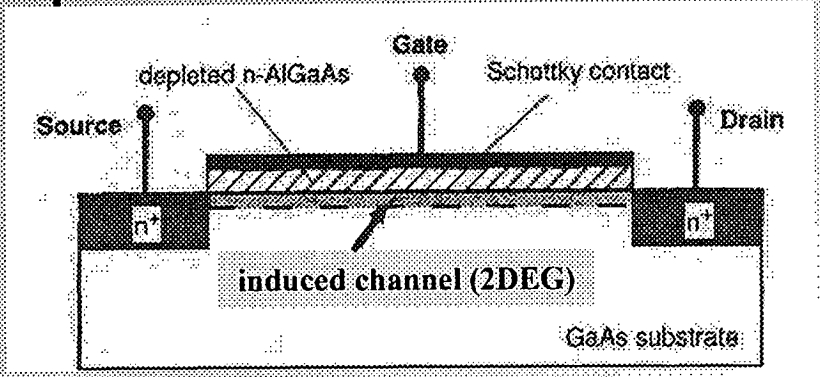
Can be extremely high for small L

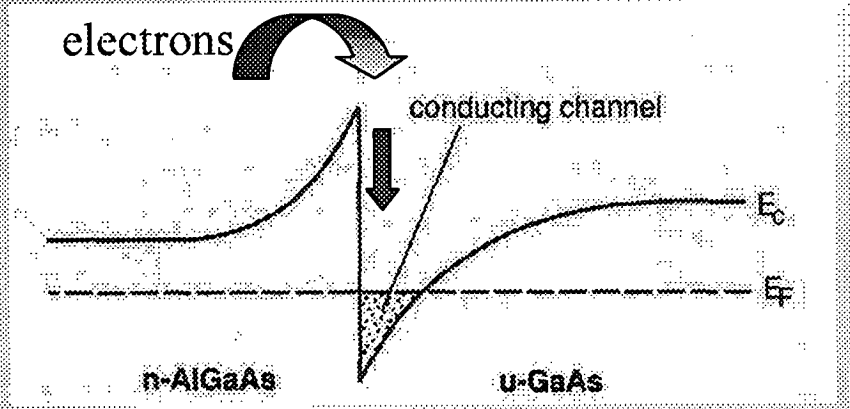
$$I = V_0\ \mu\, Z\, C_i \times (V - V_T)/L \longrightarrow I = v_S\, Z\, C_i \times (V - V_T)$$

$$v = \mu \times E \sim \mu \times V_0 / L$$

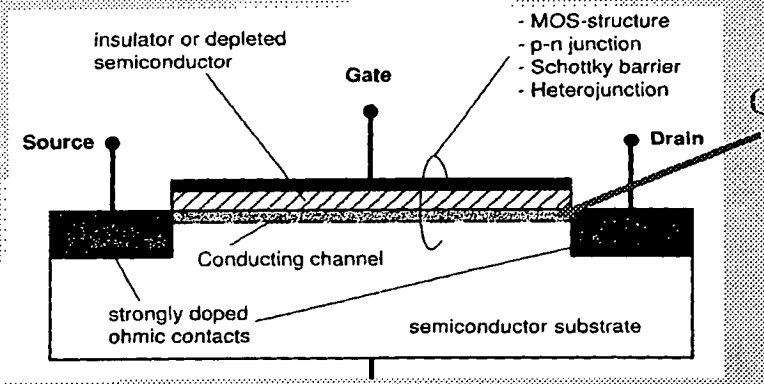
The Heterostructure Field-Effect Transistor (HFET)

The channel of HFETs is formed by 2D electron gas (2DEG)





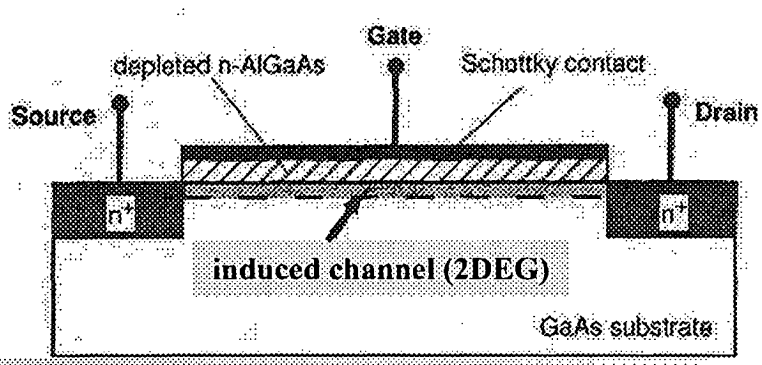
HFET

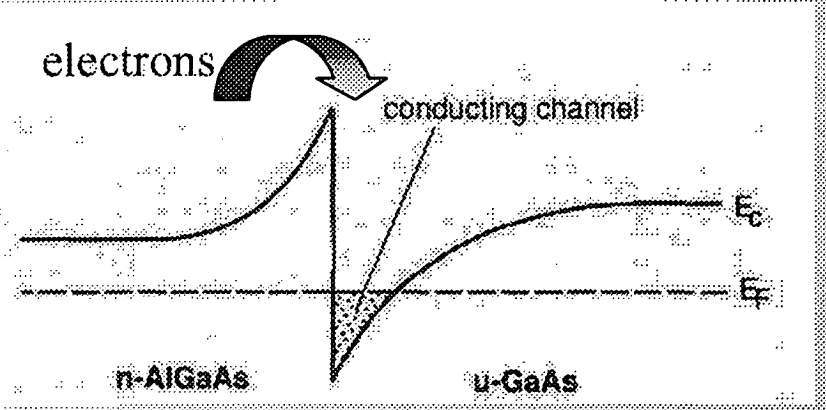


JFET, MOSFET, MESFET

The Heterostructure Field-Effect Transistor (HFET)

The channel of HFETs is formed by 2D electron gas (2DEG)





after T.A. Fjeldly, T. Ytterdal and M. Shur, 1998

Undoped active layer

Very high N_S;
very high μ;
very high v_S (in sub-μ HFETs)

1960 - Accumulation layer prediction (Anderson)
1969 - Enhanced mobility of 2DEG prediction (Esaki & Tsu)

1978 Enhanced mobility observed (Dingle et. al.)

1980 The first Heterojunction FET (HFET)
1991 The first GaN based HFET (A. Khan)